Enrollment No:-_____ Exam Seat No:-_____

C.U.SHAH UNIVERSITY

Summer-2015

Subject Code: 5TE02ADA1 **Subject Name: ARM & DSP Architecture Programming & Interfacing**

Course Name: M.Tech (EC) Date: 20/5/2015

Semester: II Marks: 70

Time: 02:30 TO 05:30

Instructions:

1) Attempt all Questions in same answer book/Supplementary.
2) Use of Programmable calculator & any other electronic instrument prohibited.
3) Instructions written on main answer book are strictly to be obeyed.
4) Draw neat diagrams & figures (if necessary) at right places.
5) Assume suitable & perfect data if needed.

SECTION – I

Q.1	(a)	State and explain in brief different conditional flags in ARM processor.	02
	(b)	Explain with example pre-index addressing in ARM processor.	02
	(c)	Explain with example UMULL and UMLAL instructions	02
	(d)	Enlist different ARM processor modes.	01
Q.2	(a)	Enlist different conditional codes for ARM processor. Explain any four with examples.	05
	(b)	Write an ALP to arrange given array of 32-bit data in ascending order.	05
	(c)	Explain with example different comparison instructions.	04
		OR	
Q.2	(a)	In ARM, explain exceptions.	05
	(b)	Write an ALP to find out the factorial of given no.	05
	(c)	Explain with example different single register data transfer load instructions.	04
Q.3	(a)	Write an ALP to add the given array of 32-bit data. Assume result is more than 3-bit.	05
	(b)	Explain with examples arithmetic instructions of ARM 7 processor	05
	(c)	Explain with diagram CPSR.	04
		OR	
Q.3	(a)	Write an ALP to find the smallest data from the given array of32-bit data.	05
	(b)	Explain with diagram interfacing of switches and relays with AT(!SAM7S ARM microcontroller	05
	(c)	Explain with examples offset addressing and post-index addressing.	04

SECTION – II

Q.4	(a)	Enlist the basic architectural features of programmable DSP devices.	02
	(b)	Explain with diagram in brief program sequencer unit of programmable DSP.	02
	(c)	What do you mean by interlocking in DSP	02
	(d)	Draw basic block diagram of Multiplier unit in DSP.	01

Q.5	(a)	Enlist basic DSP computational building blocks and explain MAC unit.	05
	(b)	Explain Hardware Looping in DSP	05
	(c)	Explain concept of on chip memory in DSP.	04
		OR	
Q.5	(a)	Explain interrupts in DSP	05
	(b)	Explain any two speed issues for programmable DSP devices.	05
	(c)	Explain with examples different general addressing modes of DSP	04
Q.6	(a)	Draw and explain functional diagram of CPU of TMS320C54xx	05
	(b)	Enlist different On-Chip peripherals of TMS5320C54xx. Explain any two of them.	05
	(c)	Explain with diagrams bus structure of Von Neumann and Harvard architectures.	04
		OR	
Q.6	(a)	Draw and explain functional diagram of barrel shifter and multiplier/adder of TMS320C54xx	05
	(b)	Explain with diagram McBSP of TMS5320C54xx.	05
	(c)	Expla with diagram address generation unit of programmable DSP.	04